Advanced
Digital Chips

An Embedded Microprocessor Company

Mar. 2007
Advanced Digital Chips (ADC), a Korean KOSDAQ company began developing a next generation CPU architecture technology in 1998.

This state of the art CPU, called EISC, is designed as a embedded MCU solution.
<table>
<thead>
<tr>
<th><strong>Company Overview</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Business Units</strong> : Semiconductor Design Company</td>
</tr>
<tr>
<td>- Multimedia/Consumer/Game</td>
</tr>
<tr>
<td>- System on Chip (SoC) ASSP Development</td>
</tr>
<tr>
<td>- Intellectual Property (IP) Licensing</td>
</tr>
<tr>
<td><strong>Location</strong> : Seoul, Korea</td>
</tr>
<tr>
<td><strong>Overseas Presence</strong> : Silicon Valley Subsidiary (March 2002)</td>
</tr>
<tr>
<td>- Pennsylvania Subsidiary (September 2003)</td>
</tr>
<tr>
<td>- China Subsidiary (April 2006)</td>
</tr>
<tr>
<td><strong>Founding Date</strong> : April 16, 1996</td>
</tr>
<tr>
<td><strong>KOSDAQ Shares</strong> : 5,200,000 Shares @ 500 won par value</td>
</tr>
<tr>
<td><strong>Employees</strong> : 75 (30 Involved in R &amp; D Related Activities)</td>
</tr>
</tbody>
</table>
### Business area

<table>
<thead>
<tr>
<th>SoC ASSP business</th>
<th>MCU IP Business</th>
<th>Trading</th>
</tr>
</thead>
</table>
| 1. Multimedia chip - graphic/video processor  
2. H.264 codec - DMB/ PMP  
3. Etc. | 1. Developing a next generation CPU architecture technology in 1998 to offer a smaller, faster and cheaper solution.  
2. ADC introduces the EISC technology to the industry in two ways, firstly through the sale of multimedia SoC incorporating the EISC MCU, and secondly by licensing its EISC MCU as IP. | AKM, RICOH’s products Trading |

**1.** Developing a next generation CPU architecture technology in 1998 to offer a smaller, faster and cheaper solution.

**2.** ADC introduces the EISC technology to the industry in two ways, firstly through the sale of multimedia SoC incorporating the EISC MCU, and secondly by licensing its EISC MCU as IP.
EISC (Extendable Instruction Set Computer) is a new ISA (Instruction Set Architecture) and computer architecture developed by ADC (Advanced Digital Chips Inc).

It combines key advantages of two leading architectures: Reduced Instruction Set Computer (or RISC) and Complex Instruction Set Computer (or CISC)
EISC is a next generation architecture that has advantages over the existing RISC and CISC architectures.
• ADC is the only house with own its proprietary commercially-proven architecture
• The EISC technology is patented in U.S., Taiwan and Korea with patents pending worldwide.
**Benchmark Results**

<table>
<thead>
<tr>
<th>Technology</th>
<th>AE32000</th>
<th>SE3208</th>
<th>ARM7TDMI</th>
<th>MIPS-R3000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Frequency</td>
<td>0.5um</td>
<td>0.5um CMOS</td>
<td>0.5um(0.35um)</td>
<td>0.5um CMOS</td>
</tr>
<tr>
<td>Code Size</td>
<td>50Mhz</td>
<td>50Mhz@5V</td>
<td>33Mhz(55Mhz)</td>
<td></td>
</tr>
<tr>
<td>Gate count</td>
<td>100</td>
<td>-</td>
<td>100</td>
<td>177.7</td>
</tr>
<tr>
<td>Power consumption</td>
<td>34K</td>
<td>20K</td>
<td>42K</td>
<td>-</td>
</tr>
<tr>
<td>Chip size</td>
<td>200mW</td>
<td>330mW(0.6mw/Mhz)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Performance</td>
<td>1000x1000(target)</td>
<td>1892x1168</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

* Better core density
* Simple Instruction set
* Smaller silicon (half that of ARM) die size, hence, cheaper.
* “Extendible” = more flexible
**EISC benefits**

### Technology Advantage - Comparison

<table>
<thead>
<tr>
<th></th>
<th>CISC</th>
<th>RISC</th>
<th>EISC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Major Features</strong></td>
<td>- for high-end computers</td>
<td>- 32-bit fixed code</td>
<td>- Post-PC Devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Scalable = 16, 32, 64 Bit Solutions</td>
</tr>
<tr>
<td><strong>Code Instruction</strong></td>
<td>Complex</td>
<td>Simple</td>
<td>Simple</td>
</tr>
<tr>
<td><strong>Relative Program Size</strong></td>
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<td>160-180</td>
<td>100</td>
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<td>Not Suitable</td>
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<td>Ideal</td>
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<td><strong>Weaknesses</strong></td>
<td>- Complex code and hardware</td>
<td>- Difficult to develop high-end MCU (64-bit and higher)</td>
<td>- Difficult to develop 16-bit MCU</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>- Not efficient for 64bit MCU</td>
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### C Object Size Comparison

<table>
<thead>
<tr>
<th>Processor</th>
<th>Alpha-RISC</th>
<th>PowerPC601</th>
<th>MIPS-R4000</th>
<th>PA-RISC</th>
<th>ARM-7</th>
</tr>
</thead>
<tbody>
<tr>
<td>EISC</td>
<td>1.00</td>
<td>1.92</td>
<td>1.46</td>
<td>2.22</td>
<td>2.23</td>
</tr>
</tbody>
</table>

Source: Company Data

**Advantage of both CISC and RISC**

1. Simple Instruction Set
2. Less Memory
3. Simple Hardware
4. Less Power

**Lower Development Cost**

Faster Time to Market

Higher Performance / $
### Embedded MCU Soft core IP

<table>
<thead>
<tr>
<th>Model</th>
<th>ALU/Data/Address</th>
<th>Address Size</th>
<th>Frequency</th>
<th>Gate Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>SE 1608</td>
<td>16 bit ALU/Data/Address</td>
<td>64K byte address</td>
<td><a href="mailto:60MHz@0.35um">60MHz@0.35um</a></td>
<td>8K Gate Count</td>
</tr>
<tr>
<td>SE 3208</td>
<td>32 bit ALU/Data/Address</td>
<td>4G byte address</td>
<td><a href="mailto:60MHz@0.35um">60MHz@0.35um</a></td>
<td>24K Gate Count</td>
</tr>
<tr>
<td>AE 32000 B/C</td>
<td>32 bit ALU/Data/Address</td>
<td>4G byte address</td>
<td>120~150 MHz @0.18um</td>
<td>46K Gate Count</td>
</tr>
<tr>
<td>AE 64000</td>
<td>64 bit ALU/Data/Address</td>
<td>4T byte address</td>
<td>100 <a href="mailto:MHz@0.18um">MHz@0.18um</a></td>
<td>140K Gate Count</td>
</tr>
</tbody>
</table>

**SE 1608**
- 16 bit ALU/Data/Address
- 64K byte address
- 60MHz@0.35um
- 8K Gate Count

**SE 3208**
- 32 bit ALU/Data/Address
- 4G byte address
- 60MHz@0.35um
- 24K Gate Count

**AE 32000 B/C**
- 32 bit ALU/Data/Address
- 4G byte address
- DSP
- FPU
- 120~150 MHz @0.18um
- 46K Gate Count

**AE 64000**
- 64 bit ALU/Data/Address
- 4T byte address
- FPU
- SIMD-DSP
- 100 MHz@0.18um
- 140K Gate Count

**8GPR/6SPR, 3 Stage Pipeline**

**16GPR/7SPR, 5 Stage Pipeline, MMU, Harvard Architecture 4 Co-Processors**

**BPR for Debug**

**On-Chip Debugger (On Silicon ICE)**

**Load-Store Instruction Set**

**16 bit Fixed Length Instruction Set & Extendable Instruction Set (LERI)**
## IP LIST

### Microprocessor
- 16bit EISC Microprocessor - SE1608A
- 32bit EISC Microprocessor - SE3208A
- 32bit EISC Microprocessor - AE32000B
- 64bit EISC Microprocessor – AE64000
- 64bit SIMD/DSP
- 64bit FPU
- Unified Cache Controller
- Harvard Cache Controller (TLB)
- Memory Management Unit
- Low power Cache Controller

### H.264 CODEC/ JPEG CODEC
- H.264 encoder/decoder
- MJPEG encoder/decoder
### Special Peripherals

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADPCM</td>
<td>ADPCM Decoding Engine (CCITT G.726)</td>
</tr>
<tr>
<td>Bit Block Transfer controller</td>
<td>Screen to screen block transfer &amp; sprite</td>
</tr>
<tr>
<td>Sound Engine</td>
<td>32 channel, 16bit, ~44.1kHz stereo PCM, 8bit, U-Law/PCM, 16bit PCM</td>
</tr>
</tbody>
</table>
| 2D Graphic based on 3D | Rotation/Zoo In-out  
|               | Texture and Tile map                                                        |
|               | Transparency, Alpha Blending                                                |
| Video Encoder | Hue Program Control, RGB to YCbCr Converter  
|               | Programmable C-Filter Bandwidth                                              |
|               | Programmable Multi-Standard Format                                          |

### Peripherals

<table>
<thead>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-INTC</td>
<td>Basic Interrupt Controller</td>
</tr>
<tr>
<td>B-TIMER</td>
<td>Basic Timer</td>
</tr>
<tr>
<td>SMC</td>
<td>Static Memory Controller</td>
</tr>
<tr>
<td>GDMAC</td>
<td>General DMA Controller</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver/Transmitter</td>
</tr>
</tbody>
</table>
## IP LIST

### Peripherals

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>PPM</td>
<td>Pulse Period Measurement</td>
</tr>
<tr>
<td>I2C</td>
<td>Inter IC Bus Controller</td>
</tr>
<tr>
<td>I2S</td>
<td>Inter IC Sound Bus Controller</td>
</tr>
<tr>
<td>WDT</td>
<td>Watch Doc Timer</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input Output Controller</td>
</tr>
<tr>
<td>PINTC</td>
<td>Priority Programmable Interrupt Controller</td>
</tr>
<tr>
<td>SIO</td>
<td>Sync. IO Bus Controller</td>
</tr>
<tr>
<td>RTC</td>
<td>Real Time Clock</td>
</tr>
<tr>
<td>Key Scan</td>
<td>Key Input Scan Controller</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface Controller</td>
</tr>
<tr>
<td>HDLC</td>
<td>High Level Data Link Controller</td>
</tr>
<tr>
<td>IEEE1284-Host</td>
<td>Parallel Bus Master Controller</td>
</tr>
<tr>
<td>IEEE1284-Device</td>
<td>Parallel Bus Slave Controller</td>
</tr>
<tr>
<td>NOR-FMC</td>
<td>Nor Type Flash Memory Controller</td>
</tr>
<tr>
<td>NAND-FMC</td>
<td>Nand Type Flash Memory Controller</td>
</tr>
<tr>
<td>PCMCIA</td>
<td>PCMCIA Host Bus Adapter</td>
</tr>
<tr>
<td>IDE</td>
<td>IDE Controller for HDD Interface</td>
</tr>
<tr>
<td>LCDC</td>
<td>Mono/STN LCD Controller</td>
</tr>
</tbody>
</table>
SoC Platform
Platform embodiment based on AMBA/AHB

- 32Bit EISC Wrapper
- External Memory Controller AHB Wrapper
- HW Module AHB Wrapper
- APB Bridge
- IntMem
- Arbiter
- Ethernet
- APB Wrapper
- HW Module
- IntMem
- Timer
- Int
1) 16Bit Embedded Board (16S310)

2) 32Bit Training Board (Jupiter)

3) 32Bit Training Board (GMX1000)

4) 32Bit Game Board (Amazon)
EISC EVM Board

1) I/O Control board for Game
2) 16bit Training Kit
3) 32bit EFT/POS Terminal board (eos)
ADC’s SoC Productions
Partnership EISC’s key strength

EISC

In partnership

adc
SoC Successful Story
(Reference Story)

EISC is a proven technology
1. Reference Story

**1. KORITECH**

- Being applied to the handy Karaoke
- A strategic product for overseas Market

**1. Enter-Tech**

- Being applied to the handy Karaoke
- Overseas export product
I. Reference Story

1. NAMCO (in Japan)
   - Being applied to the gambling game
   - Being applied to the arcade game
   - Apply to the AMAZON

2. Para Enterprise
   - Arcade Game / Gambling Game
1. VISCO (in Japan) - Arcade Game / Gambling Game

2. UNIANA - Arcade Game
5’rd SoC RobotWar competition held with EISC CPU brain board at AP SoC (Asia Pacific on Chip) 2006.
1) Taekwon Robot board
SoC TANK Robot Board

2) Tank Robot Brain Board
Jupiter - Educational Training Kit for 32bit embedded system and S/W

- Training Kit

- Educational Training Kit for 32bit embedded system and S/W

Training Book

Training Book
Training Kit

GMX1000 training board

3D animation training board

GMX1000 training kit

3D animation training kit
EISC EVM Board

1) 16Bit Embedded Board (16S310)

2) 32Bit Training Board (Jupiter)

3) 32Bit Training Board (GMX1000)

4) 32Bit 3D Game Training Board (Amazon)
1) I/O Control board for Game

2) 16bit Training Kit

3) 32bit EFT/POS Terminal board (eos)

4) 32Bit Game Board (Amazon)
I. Reference Story

License contract signed with STA in Australia. (2000.9)
Developed the Power Line Communication System Solution chip
Powerful Power Line Transceiver and control networking protocol firmware into a single chip.

License contract signed on 32bit EISC with LG Electronics (1999.11)
Developed Digital TV chip set
1. Reference Story

1. ADPCM chip
   - Being applied to the Saying book
   - Being applied to the Talking Dog
I. Reference Story

Muse2

Being applied GPS Appliance

GUGU Toy (www.구구토이.co.kr)
Multimedia processor
- Being applied to the handy Karaoke, Game and etc.
I. Reference Story

eos

Being applied to EFT/POS & PINPAD Appliance

SE16S310

USB controller with 16bit CPU.
License contract signed with Metel (2004)
Under developing wireless chip set for MP3 and mobile phone.
Under developing Active RFID reader processor

- Secured cargo visibility
- military
- Waterpark safety

Guests simply swipe their wristbands over the LocationStation’s reader to display the real-time location of each group member.
Ⅰ. Reference Story

License contract signed with **SamSung Techwin** (2005)
Being applied to high resolution CCTV camera
High resolution Day&night DSP chip

Under developing **Winner4** Project
Being applied to high resolution camera for car
High resolution Day&night DSP chip
Ⅰ. Reference Story

SDIS
(sysfo lap)

EYENIX
SAMSUNG
TECHWIN
Under develop
(sysfo lap)

3M pixel mobile camera phone chip
Being applied mobile camera phone.

Under developing 5M pixel mobile camera phone chip)
Ⅰ Reference Story

**DMB decoder**
Under develop

- Under developing DMB multimedia processor
Mixed microprocessor with OP amp
Writing with supersonic wave’s pen.
1. License contract signed on 32bit EISC with LG Electronics (1999.11)
   - Effective date: November, 2001
   - A transfer of 32bit EISC technology

2. License contract signed with STA in Australia. (2000.9)
   - Effective date: September, 2000
   - A transfer of 32bit EISC technology

   - Effective date: March, 2001
   - A transfer of 16bit EISC technology

   - Effective date: December, 2001 /May, 2002
   - A transfer of 32bit EISC technology, A transfer of 16/64bit EISC technology

5. Licensed contract with Amerix group in U.S.A (2002.3)
   - Effective date: March, 2002
   - A transfer of 16/32/64bit EISC technology (Allowance of master license)
III. Other Activities

Contribute EISC CPU to the university

Seoul Nat'l University (2002.5.7)
KAIST (2002.6.27)
ICU (2002.6.27)
Kyungho University (2002.7.24)
KJIST (2003.3)
Korea University (2003.9)
Yunsei University (2003.10)
HanYankg University (2005.5)

Contribute evaluation board to the university

Hong Ik University (2003.5)
SIPAC (2002.9)

EISC Cooperative Education

Korea Univ. (Professor Oh.)
Korea Univ. (Professor Choi.)
Yunsei Univ. (Professor Lee.)
BuKyung Univ. (Professor Cho.)
Oregon state Univ. (Professor Ben Lee)
Cheju National Univ. (Professor Lim)

Research Institute of EISC Platform and SoC Development

ETRI (Manager Cho)
KAIST SIPAC (Professor Yu)
ICU (Professor Park)
EISC Tech. Benchmarking & Biz. Strategy
Embedded Microprocessor Market

**Market Moving to 32 bit and ARM**

32 Bit Microcontroller Market

- 2001: 2.0 (Billions $)
- 2002: 3.0 (Billions $)
- 2003: 5.0 (Billions $)

System Level Design Activity

- Core based Designs %

Source: SIA, November 2000

"ARM is the leading core architecture and expected to remain number one"

Semico, January 2001

Source: Gartner Group, November 2000
### Comparison Table

#### Comparison of ARM7 with SE3208

<table>
<thead>
<tr>
<th></th>
<th>SE3208 (Jupiter)</th>
<th>ARM7TDMI</th>
<th>MIPS-R3000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 um CMOS</td>
<td>0.35 um CMOS</td>
<td>0.35 um CMOS</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>60Mhz @ 3.3V</td>
<td>55Mhz</td>
<td></td>
</tr>
<tr>
<td>Code Size</td>
<td>100</td>
<td>113.9 (ARM7:165)</td>
<td>166.7</td>
</tr>
<tr>
<td>Gate count</td>
<td>24K</td>
<td>42K</td>
<td>?</td>
</tr>
<tr>
<td>Power consumption</td>
<td>300 mW (target)</td>
<td>330mW (0.6mw/Mhz)</td>
<td>?</td>
</tr>
<tr>
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<td>1000x1000 (target)</td>
<td>1829x1168</td>
<td>?</td>
</tr>
</tbody>
</table>

*Clock frequency can be improved by customizing the cache block.*

#### Comparison of i8051 and Z80 with SE1608

<table>
<thead>
<tr>
<th></th>
<th>SE1608 (16bit)</th>
<th>i8051 (8bit MCU)</th>
<th>Z80 (8bit MCU)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate count</td>
<td>4~6K</td>
<td>8K</td>
<td>10K</td>
</tr>
<tr>
<td>Architecture</td>
<td>RISC Type</td>
<td>CISC Type</td>
<td>CISC Type</td>
</tr>
</tbody>
</table>
## Comparison Table

### Comparison of ARM9 with AE32000

<table>
<thead>
<tr>
<th></th>
<th>ARM920T</th>
<th>AE32000(Angel)</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Size</td>
<td>?</td>
<td>Good</td>
<td></td>
</tr>
<tr>
<td><strong>IPC</strong></td>
<td>0.67(ARM7=0.53)</td>
<td>0.87</td>
<td>Based on Dhrystone 2.1</td>
</tr>
<tr>
<td>Pipeline</td>
<td>5 stage pipeline</td>
<td>5 stage pipeline</td>
<td></td>
</tr>
<tr>
<td>Cache</td>
<td>Harvard architecture</td>
<td>Harvard architecture</td>
<td></td>
</tr>
<tr>
<td>MMU</td>
<td>Support</td>
<td>Support</td>
<td></td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>200MHZ(0.18(\mu))</td>
<td>120MHZ(0.18(\mu))</td>
<td>(not optimize of cache block Layout)</td>
</tr>
<tr>
<td>Area</td>
<td>2,500K Tr.</td>
<td>1,348K Tr.</td>
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## Comparison Table

### Comparison of Code Size

<table>
<thead>
<tr>
<th>Relative Code Density</th>
<th>AE32000</th>
<th>Mips-r3000</th>
<th>ARM7TDMI</th>
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<tr>
<td></td>
<td>100</td>
<td>171</td>
<td>110</td>
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</table>

- SH-3 (Hitachi) 130
- V850 (NEC) 118
- MC5200 (Motorola) 139 (coldfire)

**Platform**: Linux (Window-95/98, Window-NT)
**Compiler**: GCC-2.95.2 (FSF GNU GCC)
**Object Program**: ANSI C library programmed by Cygnus
  - C Math library programmed by Sun used at Sun workstation
  - C++ Standard Template Library by SGI used at SGI workstation

**Compiled machine code size**: 381,560 bytes at MIPS-R3000
# Technology Advantage - Comparison

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Source: Company Data
Strategy for overcoming the ARM market

Marketing Strategy of EISC CPU

1) Free offer and open to the public of compiler, development environment, source code of RTOS

2) The supply of 32bit EISC CPU board for education (Use for education of university and institute)

3) The open to the public of embedded Linux

4) Open a competitive exhibition which is included the robot football and robot war, and grant of premium and prize for the winning team

5) The joint ownership of technology through the organization of EISC CPU group
Strategy for overcoming the ARM market

Command of ARM market

Security of Market Share & Profit creation

- New market entry
- Accomplishment of Time-to-market
- Enterprise image raising Through the satisfaction Of customer’s needs

Free offer of compiler, RTOS, and development environment
EISC CPU Marketing
Various product development through the cooperation with system company
Low Cost Marketing

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Thank you...